# REASUNES

#### N Channel MOSFET

#### Applications:

- •Adapter & Charger
- •SMPS Standby Power
- •AC-DC Switching Power Supply
- •LED driving power

#### Features:

- •Low On Resistance
- •Low Gate Charge
- •Peak Current vs Pulse Width Curve
- •RoHS Compliant

Lead Free Package and Finish

| ID   | RDS(ON)(Typ.) | Vdss |
|------|---------------|------|
| 8.0A | 0.96Ω         | 600V |

2.Drain 1.Gate o T0-220F Not to Scale

Ordering Information

| Part Number | Package | Marking |
|-------------|---------|---------|
| RS8N60F     | T0-220F | RS8N60F |

#### Absolute Maximun Ratings Tc=25°C unless otherwise specified

| Symbol      | Parameter   | RS8N60F    | Units |
|-------------|---|------------|-------|
| VDSS        | Drain-to-Source Voltage (Note*1)  | 600        | V     |
| ID          | Continuous Drain Current  | 8.0        |       |
| ID@ 100 °C  | Continuous Drain Current  | 5.0        | А     |
| IDM         | Pulsed Drain Current (Note*2)   | 32.0       |       |
| DD          | Power Dissipation   | 48         | W     |
| PD          | Derating Factor above 25℃   | 0.38       | W∕℃   |
| VGS         | Gate-to-Source Voltage  | $\pm 30$   | V     |
| EAS         | Single Pulse Avalanche Engergy<br>L=30mH IAS=5.0A VDD=110V RG=25Ω TJ=25℃          | 450        | mJ    |
|             | Maximum Temperature for Soldering   |            |       |
| TL<br>TPKG  | Leads at 0.063in(1.6mm)from Case for 10<br>seconds<br>Package Body for 10 seconds | 300<br>260 | °C    |
| TJ and TSTG | Operating Junction and Storage<br>Temperature Range                               | -55 to 150 |       |

\*Drain Current Limited by Maximum Junction Temperature

Caution:Stresses greater than those listed in the "Absolute Maximum Ratings" Table may cause permanent damage to the device.

#### Thermal Resistance

| Symbol | Parameter           | RS8N60F | Units | Test Conditions  |
|--------|---------------------|---------|-------|--|
| Rejc   | Junction-to-Case    | 2.6     |       | Drain lead soldered to water<br>cooled heatsink,PD<br>adjusted for a peak junction<br>temperature of +150°C. |
| Reja   | Junction-to-Ambient | 120     |       | 1 cubic foot chamber, free air.  |

### RS8N60F

3.Source



| Symbol | Parameter                         | Min. | Тур. | Max. | Units | Test Conditions  |
|--------|-----------------------------------|------|------|------|-------|------------------|
| BVdss  | Drain-to-source Breakdown Voltage | 600  | _    |      | V     | Vgs=0V, Id=250µA |
| IDSS   | Drain-to-Source Leakage Current   |      | -    | 1.0  | μĄ    | VDS=600V, VGS=0V |
| Taga   | Gate-to-Source Forward Leakage    |      | -    | 100  | Α.    | VGS=+30V VDS=0V  |
| IGSS   | Gate-to-Source Reverse Leakage    |      |      | -100 | nA    | VGS=-30V VDS=0V  |

**OFF Characteristics** TJ=25°C unless otherwise specified

#### ON Characteristics TJ=25°C unless otherwise specified

| Symbol   | Parameter                                | Min. | Typ. | Max. | Units | Test Conditions   |
|----------|--|------|------|------|-------|-------------------|
| RDS (on) | Static Drain-to-Source On-<br>Resistance |      | 0.96 | 1.2  | Ω     | VGS=10V, ID=4A    |
| Vgs (TH) | Gate Threshold Voltage                   | 2.0  |      | 4.0  | V     | VGS=VDS, ID=250µA |

Resistive Switching Characteristics Essentially independent of operating temperature

| Symbol  | Parameter           | Min. | Тур.  | Max. | Units | Test Conditions   |
|---------|---------------------|------|-------|------|-------|-------------------|
| td(ON)  | Turn-on Delay Time  | -    | 29.00 | -    |       | Vds=300V          |
| trise   | Rise Time           | -    | 71.33 | -    | ~ C   | ID=8.0A           |
| td(OFF) | Turn-OFF Delay Time | -    | 34.93 | -    | nS    | $R_{G}=25 \Omega$ |
| tfall   | Fall Time           | _    | 32.80 | -    |       | (Note:3,4)        |

Dynamic Characteristics Essentially independent of operating temperature

| Symbol   | Parameter                      | Min. | Тур.  | Max. | Units | Test Conditions   |
|----------|--------------------------------|------|-------|------|-------|---|
| Ciss     | Input Capacitance              |      | 910   |      | pF    | V <sub>GS</sub> =0V<br>V <sub>DS</sub> =25V<br>f=1.0MHz |
| Coss     | Output Capacitance             |      | 105   |      |       |   |
| Crss     | Reverse Transfer Capacitance   |      | 2.43  |      |       |   |
| Qg       | Total Gate Charge              |      | 14.83 |      |       | VDS=480V<br>ID=8.0A<br>VGS=10V<br>(Note:3,4)            |
| $Q_{gs}$ | Gate-to-Source Charge          |      | 5.90  |      | nC    |   |
| Qgd      | Gate-to-Drain("Miller") Charge |      | 4.00  |      |       |   |



#### Source-Drain Diode Characteristics

| Symbol      | Parameter                 | Min. | Typ.   | Max. | Units | Test Conditions               |
|-------------|---------------------------|------|--------|------|-------|-------------------------------|
| Is          | Continuous Source Current |      |        | 8.0  | А     | Integral pn-diode             |
| ISM         | Maximum Pulsed Current    |      |        | 32.0 | А     | in MOSFET                     |
| Vsd         | Diode Forward Voltage     |      |        | 1.4  | V     | Is=8. 0A, V <sub>GS</sub> =0V |
| trr         | Reverse Recovery Time     |      | 520.65 |      | nS    | V <sub>GS</sub> =0V           |
| $Q_{ m rr}$ | Reverse Recovery Charge   |      | 3.72   |      | μC    | Is=8.0A, di/dt=100A/ $\mu$ s  |

#### Notes:

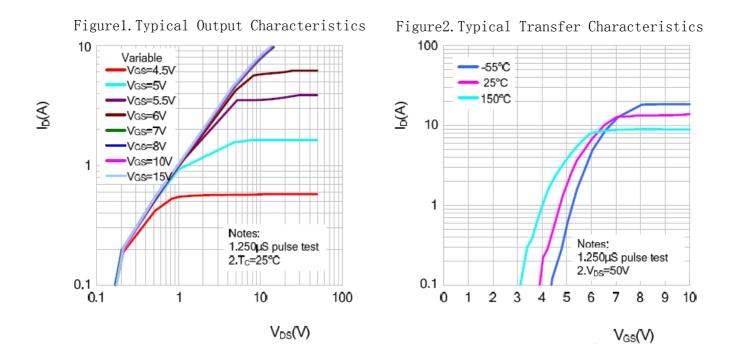
\*1.TJ=±25℃ to +150℃.

\*2. Repetitive rating; pulse width limited by maximum junction temperature.

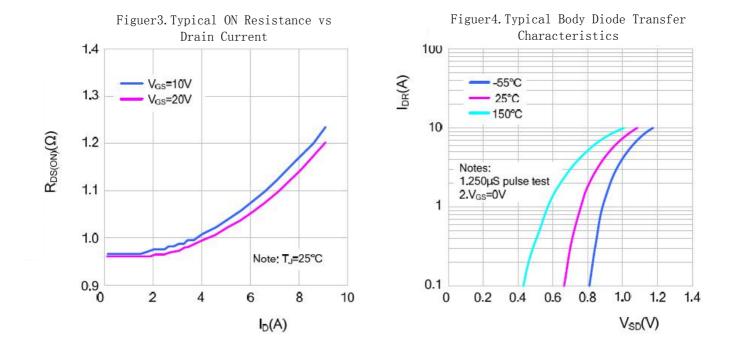
\*3. Pulse width  $\leq$  300 $\mu$ s; duty cycle  $\leq$  2%.

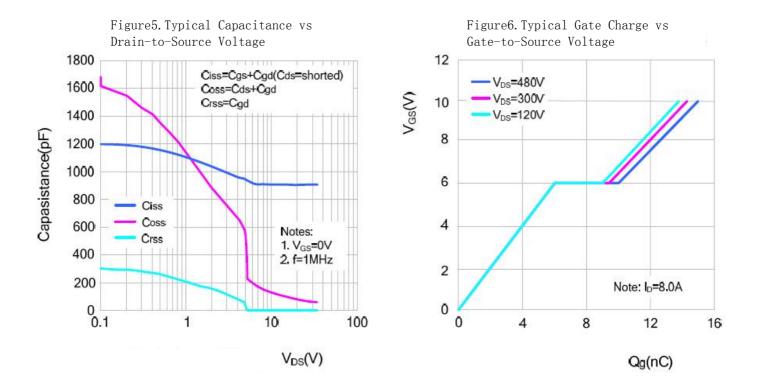
\*4. Basically not affected by temperature.

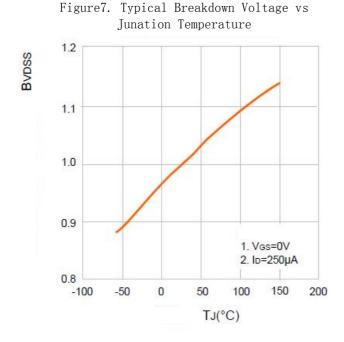
#### Typical Feature curve



## REASUNES

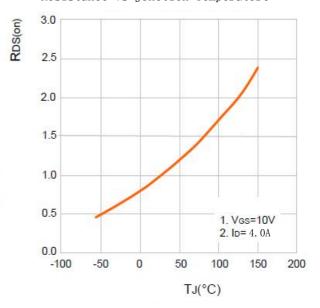


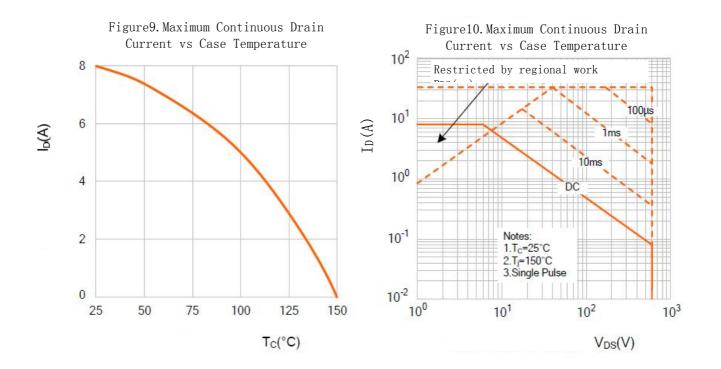




REASUNES

Figure8. Figure10.Typical Drain-to-Source ON Resistance vs Junction Temperature







#### Test Circuits and Waveforms

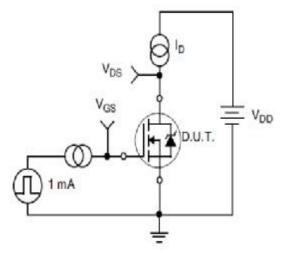


Figure11. Gate Charge Test Circuit

Vgs (TH)

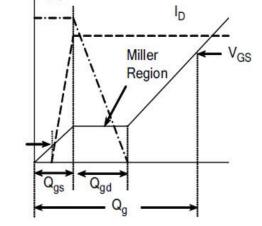
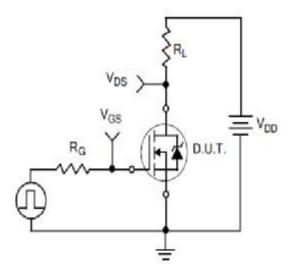


Figure12. Gate Charge Waveform

VDS



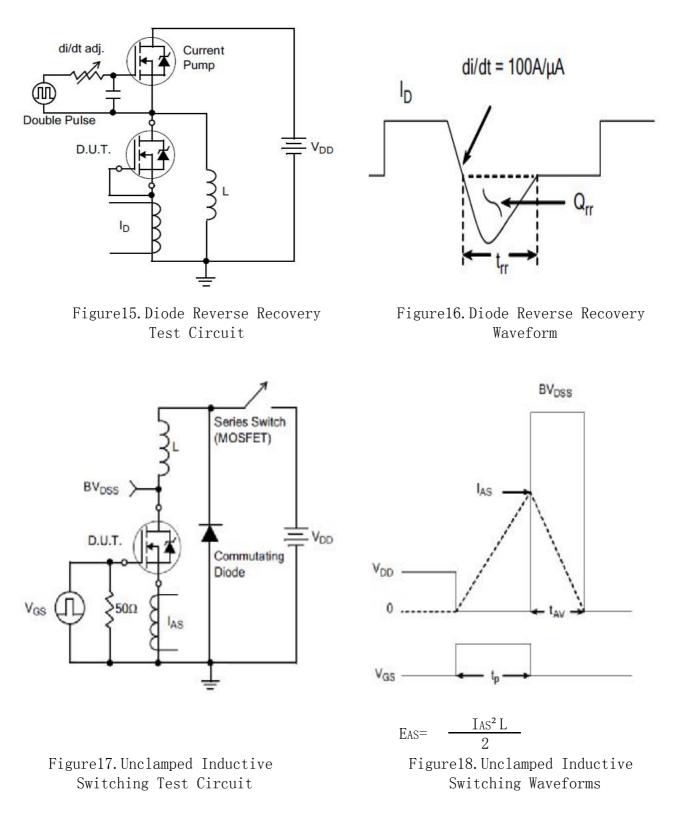
V<sub>DS</sub> 90% 10% 10% t<sub>d(ON)</sub> t<sub>rise</sub> t<sub>d(OFF)</sub> t<sub>fall</sub>

Figure13. Resistive Switching Test Circuit

Figure14. Resistive Switching Waveforms

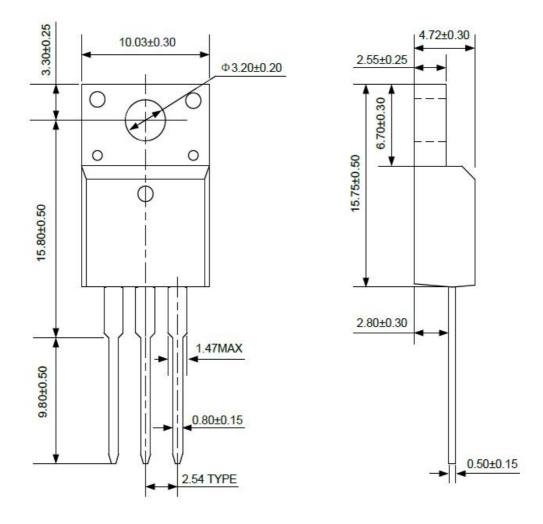


Test Circuits and Waveforms





### Package outline drawing



T0-220F



#### Disclaimers:

GuangDong Reasunos Semiconductor Technology CO.,LTD(Reasunos)reserves the right to make changes without notice in order to improve reliability, function or design and to discontinue any product or service without notice.Customers should obtain the latest relevant information before orders and should verify that such information in current and complete.All products are sold subject to Reasunos's terms and conditions supplied at the time of order acknowledgement.

GuangDong Reasunos Semiconductor Technology CO.,LTD warrants performance of its hardware products to the speciffications at the time of sale. Testing, reliability and quality control are used to the extene Reasunos deems necessary to support this warrantee. Except where agreed upon by contractual agreement, testing of all parameters of each product is not necessarily performed.

GuangDong Reasunos Semiconductor Technology CO.,LTD does not assume any liability arising from the use of any product or circuit designs described herein.Customers are responsible for their products and applications using Reasunos's components.To minimize risk, customers must provide adequate design and operating safeguards.

GuangDong Reasunos Semiconductor Technology CO.,LTD does not warrant or convey any license either expressed or implied under its patent rights, nor the rights of others. Reproduction of information in Reasunos's data sheeets or data books is permissible only if reproduction is without modification oralteration. Reproduction of this information with any alteration is an unfair and deceptive business practice. GuangDong Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such altered documentation.

Resale of Reasunos's products with statements different from or beyond the parameters stated by GuangDong Reasunos Semiconductor Technology CO.,LTD for that product or service voids all express or implied warrantees for the associated Reasunos's product or service and is unfair and deceptive business practice. GuangDong Reasunos Semiconductor Technology CO.,LTD is not responsible or liable for such statements.

#### Life Support Policy:

GuangDong Reasunos Semiconductor Technology CO.,LTD's Products are not authorized for use as critical components in life support devices or systems without the expressed written approval of GuangDong Reasunos Semiconductor Technology CO.,LTD.

As used herein:

- 1. Life support devices or systems are devices or systems which:
  - a. are intended for surgical implant into the human body,
  - b. support or sustain life,
  - c.whose failuer to when properly used in accordance with instructions for used provided in the laeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.